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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VILLECCO, JOHN M	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,679	BARNA ET AL.	
	Examiner	Art Unit	
	John M. Villecco	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14 and 29-32* is/are allowed.

6)☒ Claim(s) *15,16,18-20,24 and 26* is/are rejected.

7)☒ Claim(s) *17,21-23,25,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Regarding the 112, 2nd paragraph rejections of claims 1-14 and 31 from the previous office action, applicant has sufficiently amended claim 1 to overcome the rejection. Accordingly, the 112, 2nd paragraph rejection of claims 1-14 and 31 has been withdrawn.

2. Applicant's arguments, see page 10, line 20 to page 11, line 15, filed September 7, 2005, with respect to claim 29 have been fully considered and are persuasive. The rejection of claims 29, 30, and 32 has been withdrawn.

3. Applicant's arguments, see page 11, line 16 to page 14, line 2, filed September 7, 2005, with respect to claim 1 have been fully considered and are persuasive. The rejection of claims 1-14 and 31 has been withdrawn.

4. Applicant's arguments regarding claims 15-28 filed September 7, 2005 have been fully considered but they are not persuasive.

5. Regarding claims 15 and 26, applicant argues that "the A/D converters of Carroll are configured to be either exactly in phase, or exactly 180° out of phase, with each other ensuring that all A/Ds are either on or off simultaneously, with no staggered overlap of operating times". The examiner disagrees with this assertion. As pointed out by the applicant, the CLK-not signal for A/D's 22'' and 23'' may ***not*** be exactly 180° out of phase with the corresponding CLK signal need for A/D 22' and 23' respectively. Therefore, the A/D converters may not be exactly 180° out of phase with each other. Therefore, one of the A/D converters would start operating when a

different A/D converter is continuing to operate. For this reason, the rejection of claims 15 and 26 from the previous office action will be repeated.

6. As for claim 18, applicant argues that the circuit blocks cannot be interpreted to be the control parts as mentioned in the claim. However, the phrasing of this claim is very broad and the examiner maintains his position that Pain teaches that the plurality of control parts are individually controllable and turned off when not is use. Even if the applicant is right is asserting that the circuit blocks are the pixel rows, the examiner still believes that the circuits used for disabling the pixels can be interpreted as control parts. The load transistor (M1d) of the pixel array is individually controllable and turned off when not in use.

7. For the reasons stated above, the rejections of claims 15, 16, 18, 19, 20, 24, and 26 will be maintained.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 15, 16, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Carroll et al. (U.S. Patent No. 6,160,578).

10. Regarding ***claim 15***, Carroll discloses a high speed, increased bandwidth camera, which uses a plurality of A/D converters for processing pixels of different colors. More specifically, Carroll discloses a CCD (12), which would inherently include an array of photosensitive pixels

producing output signals indicative of values of the pixels, first A/D converters (23' and 22''), which receive a first color (green), and second A/D converters (23'' and 22'), which receive a second color (red and blue). See Figure 3. Additionally, Carroll discloses that a programmable phase shifter (26) operates to provide staggered operation timings to each of the A/D converters. In column 10, line 39 to column 11, line 32, Carroll discloses that each of the A/D converters has it's own phase that is independently adjustable using the variable phase shift circuits (85-88). Therefore, since each of the A/D converters (22', 22'', 23', and 23'') are operated at independently different phases it follows that one of the A/D converters would inherently by started when a different one of the A/D converters is operating.

11. As for ***claim 16***, as mentioned above, A/D converters (23' and 22'') receive the green pixel signals and A/D converters (23'' and 22') receive the red and blue color pixels.

12. ***Claim 26*** is considered substantively equivalent to claim 15. Please see the discussion of claim 15 presented above.

13. **Claims 18 and 19, are rejected under 35 U.S.C. 102(b) as being anticipated by Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999).**

14. Regarding ***claim 18***, Pain discloses a CMOS image sensor designed to be ultra-low power, miniature, and integrated on a single chip. The CMOS includes a two-dimensional array of photosensitive pixels and timing and control logic. See Figure 1 and page 1, section 2. Furthermore, on page 4, section 4, titled "Chip Power Dissipation" discloses that the power is

conserved by turning off the current flowing to circuit blocks that are not in used. The circuit blocks are interpreted to be the control parts.

15. As for ***claim 19***, Pain discloses the use of a voltage clamp that can be turned off when not in use. More specifically, Pain discloses in Figure 5 the use of voltage clamps to operate the A/D converters. As mentioned above, Pain discloses on page 4, section 4, titled "Chip Power Dissipation" discloses that the power is conserved by turning off the current flowing to circuit blocks that are not in used.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999) in view of Guerrieri et al. (U.S. Patent No. 6,233,012)**.

18. Regarding ***claim 20***, as mentioned previously in the discussion of claim 18, Pain discloses all of the limitations of the parent claim. However, Pain fails to specifically disclose that the column readout part includes an element that minimizes a stray capacitance. Guerrieri, on the other hand, discloses that it is well known in the art to provide an element that minimizes stray capacitance in CMOS imagers. More specifically, in order to counter the metal line

capacitance generated by the input line (212), a conductive shield line (218) is formed beneath the input line (212). See column 3, line 60 to column 4, line 30. Parasitic input capacitance slows the readout time and reduce or increases the amount of charge provided to the amplifier (col. 1, lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a structure to reduce the stray capacitance on the readout line of Pain so that readout time is not slowed.

19. **Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. ("A Low-Power Digital Camera-on-a-Chip Implemented in CMOS Active Pixel Approach", IEEE International Conference on VLSI Design, Jan. 1999)**.

20. Regarding ***claim 24***, as mentioned above in the discussion of claim 18, Pain discloses all of the limitations of the parent claim. However, Pain fails to explicitly disclose that the timing and control logic produces a converter reference voltage, a clamped voltage, and a common mode feedback voltage. However, Official Notice is taken as to the fact that it is well known in the art that CMOS image sensors include timing and control logic to generate converter reference voltages, clamped voltages, and common mode feedback voltages. These voltages are common voltages associated with the readout of the pixel signals. Furthermore, applicant seems to even admit that the generation of the voltages is typical on page 8, paragraph 0052 of the specification. Therefore, since there voltages are common in the operation of an APS CMOS image sensor, it would have been obvious to include these voltages in the APS imager of Pain.

Allowable Subject Matter

21. Claims 17, 21-23, 25, 27, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 17, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the A/D converter are successive approximation A/D converters.

With regard to claim 21, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the element includes an optimized gain element with first and second unity gain buffers, and a gain stage, said first and second unity gain buffers isolating the gain stage from the readout bus.

As for claim 22, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the control part includes a controllable bias element which is turned off to remove said bias when not in use.

Regarding claim 25, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that each of the converter reference voltage, clamped voltage, and common mode feedback voltage are produced by separate, controllable sources, which are turned off when not in use.

As for claim 27, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the second timing is 50 percent of the way through a conversion cycle represented by the first timing.

With regard to claim 28, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the A/D converting comprises successive approximation A/D converting.

23. Claims 1-14 and 29-32 are allowed.

24. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the primary reason for allowance is that the prior art fails to teach or reasonably suggest that each of the column readout part, said gain stage, and said output driving stage include at least one element which optimizes a power consumption of the stage independent of other stages.

As for claim 29, the primary reason for allowance is that the prior art fails to teach or reasonably suggest turning off the bias electrical signals at times during the acquiring of image signals when the biases are not needed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (571) 272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John M. Villecco
January 17, 2006

NGOC-YEN VU
PRIMARY EXAMINER